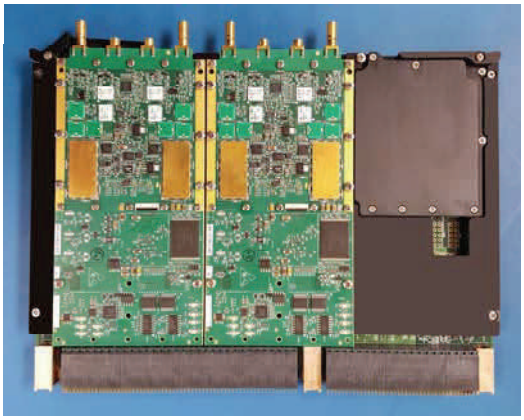
SOF ES Signal Processing Receiver (SPR) XMCs

IF, DF and AIS Receiver Mezzanines For SOF ES Systems

Key Features

- **Dual Wideband IF ES Receiver:**
  - **Two Channels of > 1 GHz BW**
- **ADF Receiver:**
  - **Provides bearings from up to 8 DF antennas, correlates to multiple IF Receivers (e.g. from Dual IF Receiver)**
- **AIS/IF ES Receiver:**
  - **Dual Band AIS Receiver**
  - **Single Channel of 1GHz BW**
- **Custom IF/RF Mezzanine Design Services**
  - **Customization of above XMCs**
  - **Porting ES/AIS algorithms to existing hardware**

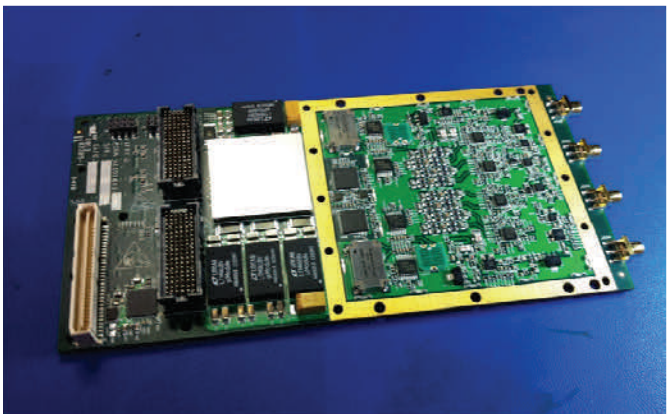


Two SPR XMCs on a VPX Carrier Card

Overview:

The Signal Processing Receiver XMCs (SPRs) are a family of mezzanines that form the core elements of the Aeronix SOF ES (Electronic Support) systems. They combine an application-tailored IF/analog signal conditioning front end with a common FPGA-based backend which provides custom digital signal processing to perform the desired ES (and/or AIS) functions.

These mezzanines represent the next step in evolution from the Copperfield 2 series of modular ESM receivers originally developed for the Naval Research Laboratory for use in RADAR surveillance applications.



AIS/IF Receiver XMC

Mezzanine Architecture

Each SPR Mezzanine Card contains a custom analog/IF front end and a common digital back end. There are 3 receiver models currently available:

- Dual IF ES Receiver, each with > 1GHz BW
- ADF Receiver/Correlator
- Combined Dual Band AIS Receiver/Single IF ES Receiver

Although the analog/IF front ends are tailored for their purpose, they can be altered to suit specific needs. In addition, the algorithms performed by the highly capable FPGA in the digital back end can also be similarly customized - contact us for more details.

Signal Processing Receiver (SPR) Specifications

IF Receiver Specifications (Dual IF or IF half of AIS/IF SPR)	
Frequency	L Band/1 GHz CF
Instantaneous Bandwidth:	> 1GHz
Frequency Resolution:	10 KHz
Instantaneous Dynamic Range:	> 50 dB
Sensitivity:	< -60dBm
Attenuation:	0-31dB
Timing:	
TOA/PW:	8nsec Resolution, 50nsec minimum PW
PRF:	> 1MHz per band
Inputs:	IF Inputs (2) Blanking (8)
Outputs:	PDWs over x4 PCIe Gen 2 IF Auxiliary (2)

ADF Receiver Specifications	
Bearing Resolution:	Contact for details; export restrictions may apply
Timing:	
TOA/PW:	8nsec Resolution, 50nsec minimum PW
PRF:	>> 1MHz
Inputs:	Up to 16 Analog inputs from up to 8 DF antennas
Outputs:	PDWs with bearings over x4 PCIe Gen 2

AIS/IF Receiver Specifications	
IF ES Band Specifications:	See IF Receiver band specs
AIS/VHF IF Coverage:	125-250MHz
UHF Coverage:	Selectable 250-375 or 375-500MHz
AIS IF Sensitivity:	< -110 dBm
Instantaneous Dynamic Range:	> 50 dB
Attenuation:	0-31 dB
Timing:	
TOA/PW:	8nsec Resolution, 50nsec minimum PW
PRF:	> 1MHz or more
Inputs:	IF Wideband for ES AIS (VHF) IF and UHF IF Blanking (8)
Outputs:	PDWs, AIS messages/samples over x4 PCIe Gen 2 IF Auxiliary (1)

Other Common Features (All SPRs):	
Common I/O:	10MHz, 1PPS, RS422/232 Serial
BIT:	Test sources at IF/RF and Digital
Connectors:	IF I/O: MCX-F DF: Omnetics 65-pin Bilobe connector All: XMC/PMC standard connectors
Mechanical:	149mm x 74mm x 13.5mm standard XMC
Power:	< 18 Watts, VPWR (+5 or +12V), 3.3V, 3.3V Aux

Note: Contact Aeronix for further details on specifications; certain export restrictions may apply

www.aeronix.com

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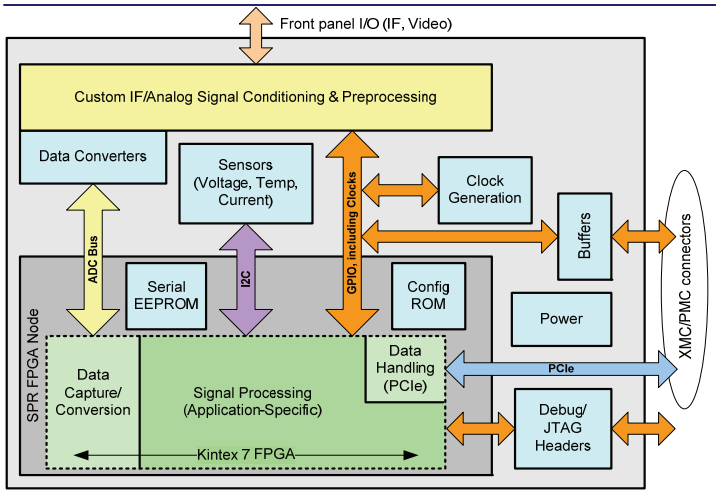
IF, DF and AIS Receiver Mezzanines For SOF ES Systems



SPR Mezzanine Common Architecture and Digital Back End

As shown in the diagram to the left, each SPR Mezzanine consists of a common digital back end fitted to a custom IF/analog signal conditioning front end. The major features of the digital back end include:

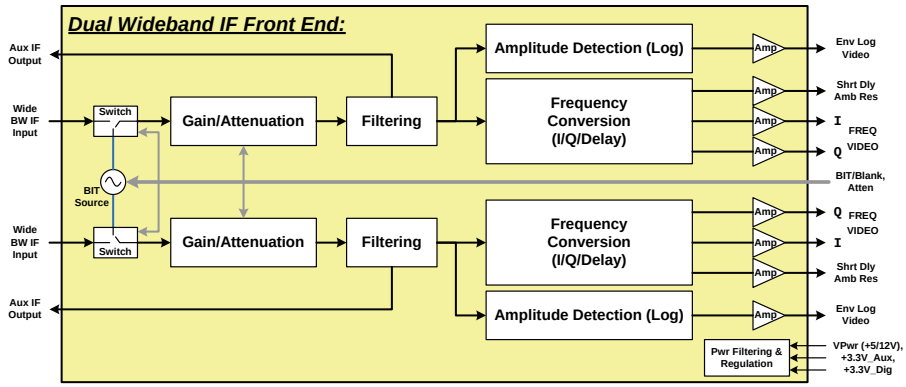
- Large, highly capable Kintex 7 FPGA
  - Built-in support for PCI Express Interface
  - Significant resources (memory and logic)
  - Proprietary signal processing algorithms developed and refined over multiple generations
- High speed ADC interfaces
- Deep configuration FLASH, ability to reload algorithms over PCIe
- Synchronizes to common 10MHz reference

There are 3 receiver functions currently available (see below). Combination of the these functions or additional signal processing functions are also feasible - contact us for more details

Dual Wideband IF Receiver Mezzanine —>

Two fully featured ES Receiver Bands. Major features:

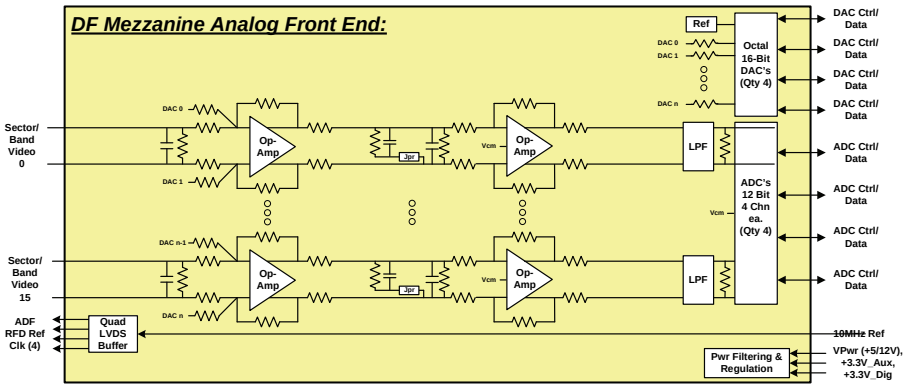
- Each ES Receiver Band:
  - > 1GHz instantaneous BW
  - Signal amplification and selectable attenuation
  - IF divided into two paths:
    - Amplitude: IF converted to log envelope
    - Frequency: IF converted to I/Q
  - BIT signal injection for verification/characterization
  - Back end digitizes amplitude/frequency , detects pulses, sends Pulse Descriptor Words (PDWs) over PCIe



ADF Mezzanine —>

Computes pulse bearings using amplitude differences from array (antenna) elements. Major features include:

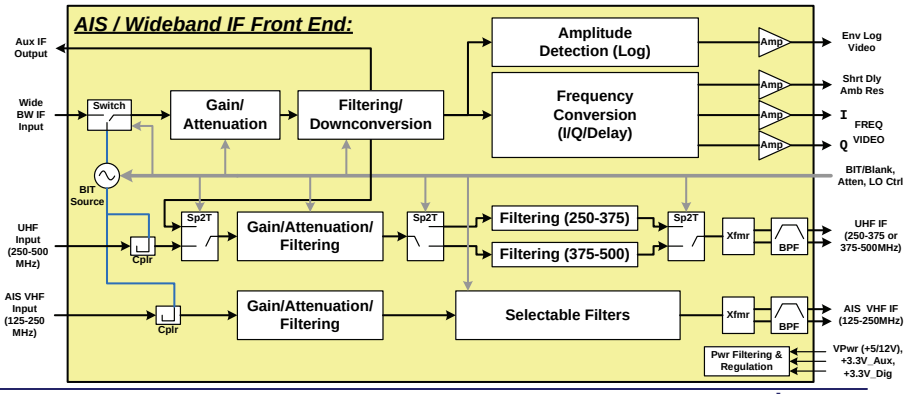
- Receives up to 16 analog signals :
  - Each analog input is amplitude (envelope-detected) output from an ADF array antenna; one or more inputs per antenna depending on configuration
  - Highly configurable buffers/filters for each
- BIT signal injection for verification/characterization
- Back end quantizes amplitude from each antenna, computes bearings, correlates IF Receiver band pulses IF , sends resulting bearing-enhanced PDWs over PCIe



AIS / Wideband IF Receiver Mezzanine —>

Combination AIS and ES Receiver. Major features include:

- 1 AIS Dual Band receiver, each band including:
  - Selectable Bandwidths
  - NMEA formatted AIS messages with timestamps
  - AM/FM demodulation, I/Q Streams
- 1 VHF Band, 250-500MHz range, divided into 2 bands
  - Wide BW IF can be downconverted for this band
  - Direct digital sampling/processing of one band
- 1 fully featured ES Receiver band, capabilities as listed under Dual Wide Bandwidth IF Receiver Mezzanine
- PDWs/AIS Messages / Streams transmitted over PCIe
- BIT signal injection for verification/characterization



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